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Indian Standard
GRAPHICAL SYMBOLS USED IN ELECTROTECHNOLOGY
PART XXIV BINARY LOGIC ELEMENTS

(First Reprint JUNE 1996)

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Indian Standard

GRAPHICAL SYMBOLS USED IN ELECTROTECHNOLOGY

PART XXIV BINARY LOGIC ELEMENTS

0. FOREWORD

0.1 This Indian Standard (Part XXIV) was adopted by the Indian Standards Institution on 6 June 1980, after the draft finalized by the Basic Standards on Electronics and Telecommunication Sectional Committee in consultation with the Semiconductor Devices Sectional Committee had been approved by the Electronics and Telecommunication Division Council.

0.2 The symbols and descriptions in this standard have been prepared with a view to electrical applications, but the majority of them may also be applied to non-electrical systems (for example, pneumatic, hydraulic or mechanical, etc).

0.3 In the preparation of this standard assistance has been derived from the following:

a) IEC Publication 117-15 First edition (1972) Recommended graphical symbols, Part 15: Binary Logic Elements. International Electrotechnical Commission.

b) BS 3939 : Section 21 Graphical symbols for electrical power, telecommunications and electronics diagrams, Section 21 Binary logic elements. British Standards Institution.

0.4 A series of Indian Standards has been prepared to standardize various graphical symbols as used in electrotechnology. The list of these standards has been given on P 39.

1. SCOPE

1.1 This standard (Part XXIV) lays down graphical symbols for binary logic elements, graphical functional symbols and some drawing rules for diagrams of binary devices.

1.2 This standard does not include the fields of analogue and hybrid computation.

2. TERMINOLOGY

2.0 For the purpose of this standard, the following definitions shall apply.

2.1 Logic Function — A combinative, storage, delay or sequential function expressing a relationship between signal input(s) and the resultant output(s).

2.2 Pure Logic Symbol — The graphical representation in diagrammatic form of a logic function.

2.3 Pure Logic Diagram — A diagram which depicts logic functions, and which consists primarily of logic symbols used to depict all logic relationships as simply as possible, without reference to physical implementation.

2.4 Logic Diagram — A diagram that depicts by logic and other symbols of distinctive shape and supplementary notations the details of signal flow and control, but not necessarily the point-to-point wiring.

Note — Logic symbols may be used to represent logic functions on circuit diagrams where pin numbers and symbols for socket locations, test points and other physical elements may be shown. In such cases, suitable annotation of the logic symbols may be included to indicate the type of element used for the physical implementation of the function.

2.5 Binary Digital Variable — A variable which may take up either one of two discrete values.

2.6 States of a Digital Variable — The two values of a binary digital variable are assigned logic states which may be represented by any two arbitrary symbols. It has become usual to use the symbols 0 and 1 for this purpose.

Note — A binary digital variable may be conveniently equated to any physical quantity for which two discrete levels can be defined.

2.6.1 The levels of the physical quantity can be expressed by:

a) Numbers, representing the measured values of the quantity corresponding to each level. Since, in practice, each level represents a range of values between defined limits, it is customary to allocate a representative number to the nominal value of each level. The representative numbers for the two nominal value are referred to as 'logic levels'.

b) Symbols, indicating the mutual relationship of the logic levels. In particular, H is often used for the level with the more positive algebraic value, and L for that with the less positive value.

c) Any two arbitrary symbols. The relationship between the two levels of the physical quantity and the logic states assigned to them is arbitrary. Their correspondence may be defined in different ways.

2.7 Binary Digital Element (Logic Element) — A binary digital element (logic element) is an element whose input and output quantities represent binary digital variables and whose outputs are defined digital functions of the inputs.

2.8 Logic Convention — A binary digital element is a physical entity and the functions it performs are established in terms of the logic levels of its inputs and outputs. Before these functions can be defined in terms of binary digital variables the relation between the physical input and output quantities, and the corresponding variables should be defined.

2.8.1 *Positive Logic Convention* — In positive logic the H (high) level of a physical quantity represents the 1-state of a binary digital variable and the L (low) level the 0-state.

2.8.2 *Negative Logic Convention* — In negative logic the H (high) level of a physical quantity represents the 0-state of a binary digital variable and the L (low) level the 1-state.

3. COMPOSITION OF THE SYMBOLS AND RULES FOR THEIR USE

3.1 The following rules are applicable to all the symbols in this standard.

3.1.1 *Composition of the Symbols for Digital Elements* — A symbol comprises:

a) An outline.

b) A qualifying symbol denoting the function.

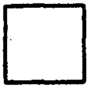
NOTE — This is a symbol which specifies the required logic operation. In certain cases this symbol is replaced or completed by numerical values necessary to define the function of the element. This symbol and/or these numerical values are drawn in the interior of the outline. For an example of application, see **3.3**.

c) Indicators for inputs and outputs.

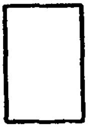
NOTE — These indicators relate to each of the inputs and outputs against which they appear. They shall be placed as defined in 4.

3.2 Logic Element

General Symbol



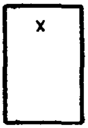
or



NOTE — The length-width ratio of the rectangle is arbitrary.

3.3 Position of the Qualifying Symbol for the Function

3.3.1 The qualifying symbol for the function is placed either in the top centre of the outline or in its centre.



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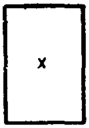
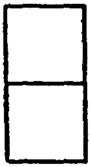


3.3.2 Additional information, for example, type, function or location of the element, may be written inside the outline of the symbol below or following the qualifying symbol.

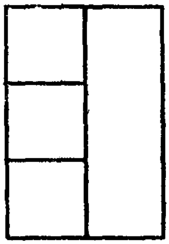
3.4 Combination of Symbols

3.4.1 To reduce the space required on the diagram, separate symbols for basic operations may be joined together but the following rules shall be observed if there is only one direction of information flow within the combination of elements.

3.4.2 There is no logic connection when the line common to two symbols is in the direction of information flow.

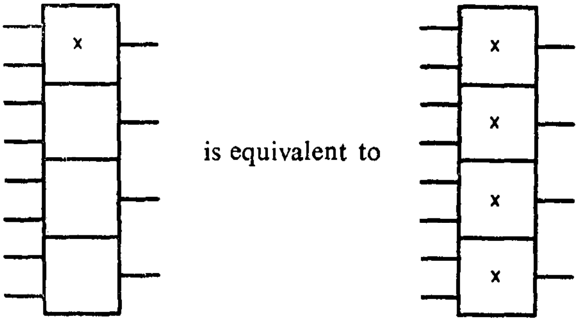


3.4.3 There is a single logic connection, without logic negation, when the line common to two symbols is perpendicular to the direction of information flow.



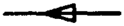
3.5 Arrays of Elements — In an array of elements having the same qualifying symbol it is sufficient to show the qualifying symbol in only one of the elements, preferably in the first or last.

Example:



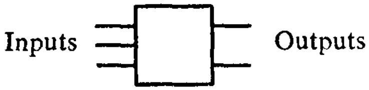
3.6 Direction of Information Flow — In principle, the direction of information flow should be from left to right and from top to bottom.

If this is not possible and the direction of information flow is not obvious then lines carrying information may be marked with an arrow-head which shall not be placed adjacent to the logic symbol.



4. INPUTS AND OUTPUTS

4.1 General — The input and output connections to the symbol are preferably placed on opposite sides of the symbol. Inputs and outputs shall never be placed on the same side of the symbol.



NOTE — A logic symbol may have any number of inputs and outputs provided that the symbol definition requirements are met.

4.2 Polarity

4.2.1 *Introduction* — Consider, for example, a circuit whose output (F) is a function of two variables (A, B), and whose output and input levels are capable of assuming only +2V and −3V. Assume that the circuit behaves according to the following table of combinations:

Inputs		*Outputs*
A	B	F
−3V	−3V	−3V
−3V	+2V	−3V
+2V	−3V	−3V
+2V	+2V	+2V

The function perfomed by an element which behaves according to the above table of combinations will depend on the choice of logic convention applied at its inputs and outputs as explained in **4.2.2**, **4.2.3**, and **4.2.4**.

4.2.2 *Positive Logic*

4.2.2.1 In positive logic, the −3V (less positive) level is the 0-state and +2V (more positive) is the 1-state.

4.2.2.2 Substitution of the logic states for the voltage levels results in the following table:

Inputs		*Outputs*
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

4.2.2.3 This is the table of combinations for an AND function. Therefore, the circuit is said to perform the AND operation.

4.2.3 *Negative Logic*

4.2.3.1 In negative logic, the –3V (more negative) level is the 1-state and +2V (less negative) is the 0-state.

4.2.3.2 Substitution of the logic states for the voltage results in the following table:

Inputs		*Outputs*
A	B	F
1	1	1
1	0	1
0	1	1
0	0	0

4.2.3.3 This is the table of combinations for the OR function. Therefore, the circuit is said to perform the OR operation.

NOTE 1 — The voltage levels used in the above table of combinations and truth tables are examples only. Absolute potentials may be positive or negative and the criterion determining the logic polarity is as follows:

a) The polarity is positive if the 1-state is represented by a *more positive* potential than the 0-state.

b) The polority is negative if the 1-state is represented by a *less positive* potential than the 0-state.

NOTE 2 — 'a more positive level' is also understood as 'less negative level' and *vice-versa.*

4.2.4 *Duality*

4.2.4.1 As shown by **4.2.2** and **4.2.3** above, a single circuit can perform either the AND operation or the OR operation. This duality has been employed in numerous single-device systems.

4.2.4.2 Given a physical device characterized by a table of combinations, the logic function performed by the device is determined by the specified choice of the 1-state at its inputs and outputs.

4.2.4.3 Each choice of the 1-state at each input and each output of a logic circuit shall be specified on the logic diagram in a manner which correctly represents the logic function designed by the logic designer.

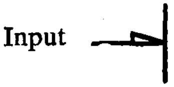
4.2.4.4 This can be done in either of the following ways:

a) The logic diagram includes a statement as to whether positive or negative logic is used. In this case the polarity indicator shall not be used, the negation indicator is used where necessary.

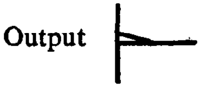
b) At each input and each output of each logic element on the diagram, the choice of the less positive level as the 1-state is specified by means of the polarity indicator shown below. The absence of the polarity indicator then indicates that the 1-state is the more positive level. In this case the negation indicator shall not be used.

4.2.5 *Polarity Indicator*

4.2.5.1 The 1-state is the less positive level, that is, negative logic is in force at this point.



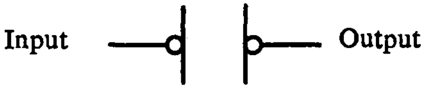
(a)



(b)

4.3 Negation — The state of the logic variable at an input or output is reversed if the logic negation indicator is applied.

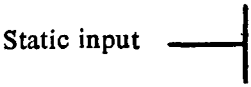
Logic negation indicator.



NOTE — If desired the connection line may be drawn through the circle.

4.4 Static and Dynamic Inputs

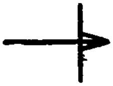
4.4.1 *Static Input* — A static input is one such that the 1-state is defined as the presence of a particular logic level, and the 0-state as the presence of the other logic level.



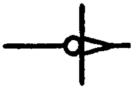
4.4.2 *Dynamic Input*

4.4.2.1 A dynamic input is one such that the 1-state is defined as the transition from a particular logic level to the other logic level, and not by the presence of one of these logic levels.

4.4.2.2 Dynamic input for which the dynamic 1-state is defined by the transition from the static 0-state to the static 1-state, is as indicated below:

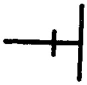


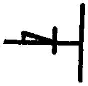
4.4.2.3 Dynamic input for which the dynamic 1-state is defined by the transition from the static 1-state to the static 0-state, is as indicated below:



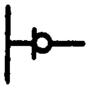
4.5 Inhibiting and Negated Inhibiting Inputs

4.5.1 *Inhibiting Input* — An inhibiting input of a digital element standing at its defined 1-state prevents the output variable of that element from standing at its defined 1-state (or its 0-state if the output is negated) whatever the value of the other input variable; when the inhibiting input stands at its 0-state the qualifying symbol of the element applies to those inputs which are neither inhibiting inputs nor negated inhibiting inputs.





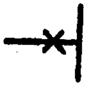
4.5.2 *Negated Inhibiting Input* — A negated inhibiting input of a digital element standing at its 0-state prevents the output variable of that element from standing at its defined 1-state (or its 0-state if the output is negated), whatever the value of the other input variable; when the negated inhibiting input stands at its defined 1-state the qualifying symbol of the element applies to those inputs which are neither inhibiting inputs nor negated inhibiting inputs.



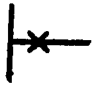
4.6 Other Inputs and Outputs

4.6.1 Line not carrying logic information.

a) Input which does not carry any logic information.



b) Output which does not carry any logic information.

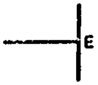


Note — These symbols may be replaced by any indicator which does not convey any logic information.

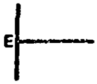
4.6.2 *Extension* — An extender element serves to extend the number of inputs of a logic element having extension facility.

The levels appearing on the extension connections are normally different from those appearing on connections between logic elements on the diagram.

a) Extension input.



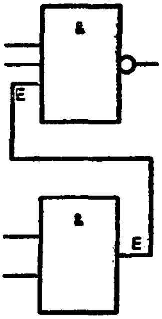
b) Extension output.



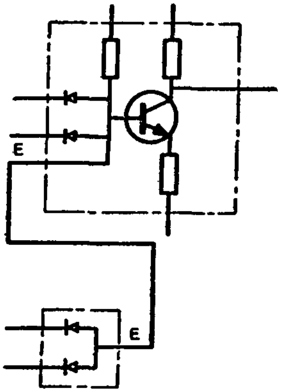
NOTE — Designation of the output may be omitted if no ambiguity arises.

Example:

Extended Nand



Explanatory diagram



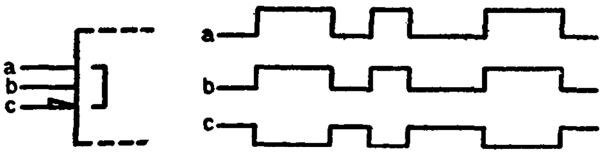
NOTE — The qualifying symbol '&' is put in both basic symbols.

4.6.3 *Two or More Lines Carrying the Same Bit of Information* — When it is required to show an input by means of several distinct lines which are related such that if one of the inputs changes, the others invariably change their states, these lines may be represented grouped by this symbol.

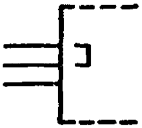
Symbol for the grouping of lines carrying the same bit of information:

Example:

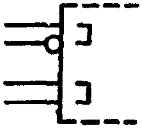
a)



b) Element with two inputs, one of which consists of two lines carrying the same bit of information.



c) Element with two inputs, each consisting of two lines carrying the same bit of information.



5. COMBINATIVE ELEMENTS

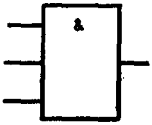
5.1 General — The basic rule for the application of the qualifying symbol denoting the function of the element is as follows:

The qualifying symbol for the element is a symbol generally indicating the number of inputs which shall necessarily take the defined 1-state to cause the output to take on its defined 1-state, provided the output is not negated.

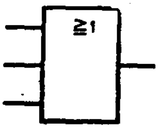
This section gives the most currently used logic elements and shows also how to apply this rule. Subject to this rule any other symbols may be developed.

5.2 Elementary Combinative Elements

5.2.1 *AND* — The output will stand at its defined 1-state if, and only if, all of the inputs stand at their defined 1-states.

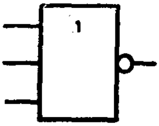


5.2.2 *OR* — The output will stand at its defined 1-state if, and only if, one or more of its inputs stand at their defined 1-states.



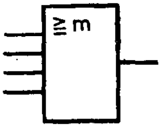
Note — '≥ 1' may be replaced by '1' if no ambiguity arises.

5.2.3 *NOT, NEGATER* — The output will stand at its 0-state if, and only if, the input stands at its defined 1-state.



5.3 Complex Combinative Elements

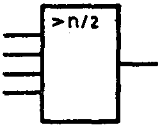
5.3.1 *Logic Threshold* — The output will stand at its defined 1-state if and only if, the number of inputs which stand at their defined 1-states reaches or exceeds the number (m) specified in the qualifying symbol.



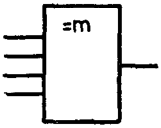
Note 1 — m shall always be smaller than the number (n) of inputs.

Note 2 — ⩾m may be replaced by m if no ambiguity exists.

5.3.2 *Majority* — The output will stand at its defined 1-state if and only if, the majority of the inputs stand at their defined 1-states.

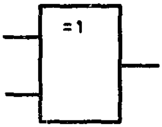


5.3.3 *m and Only m* — The output will stand at its defined 1-state if and only if, *m* and only *m* of its n inputs stand at their defined 1-states.

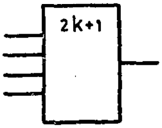


Note — *m* shall always be smaller than the number (n) of inputs.

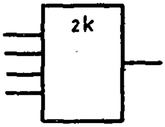
5.3.4 *Exclusive OR* — The output will stand at its defined 1-state if one, and only one of the inputs stands at its defined 1-state.



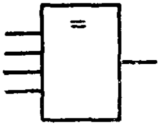
5.3.5 *Addition Modulo 2 (Odd Element)* — The output will stand at its defined 1-state if and only if, an odd number (1, 3, 5, etc) of inputs stand at their defined 1-states.



5.3.6 *Addition Modulo 2 (Even Element)* — The output will stand at its defined 1-state if and only if, an even number (0, 2, 4, etc) of inputs stand at their defined 1-states.

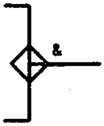


5.3.7 *Logic Identity* — The output will stand at its defined 1-state if and only if, all of the inputs stand at their defined 1-states or if none of the inputs stand at their defined 1-states.

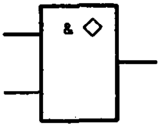


5.4 Other Combinative Elements — A distributed connection is a connection of outputs of a certain number of elements that are joined together to achieve the effect of an AND/OR operation without the use of an explicit element.

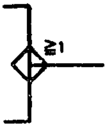
5.4.1 *Distributed AND Connection (wired AND)*



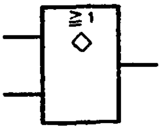
or



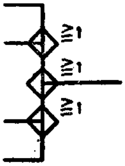
5.4.2 *Distributed OR Connection (wired OR)*



or



5.4.3 *Combination of Several Distributed OR Connections*



Notes concerning symbol numbers **5.4.1**, **5.4.2** and **5.4.3**.

NOTE 1 — The lines need not be extended into the diamond.

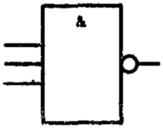
NOTE 2 — The qualifying symbol for OR or AND may be repeated at the output of preceding symbols, and other places where applicable.

NOTE 3 — The indication of the distributed (wired) connection at the symbol may be assumed to be that of an OR if no qualifying symbol is shown.

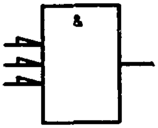
NOTE 4 — The symbol '⩾ 1' may be replaced by '1' or omitted if no ambiguity exists.

5.5 Examples of the use of Combinative Elements

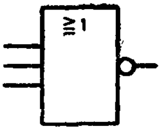
5.5.1 *And with Negated Output (NAND)* — The output will stand at its 0-state, if all the inputs stand at their defined 1-states.



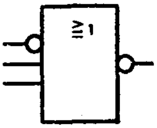
5.5.2 *AND with Polarity Indicators at the Inputs* — The output will stand at its more positive level if and only if, all the inputs stand at their less positive level. (The defined 1-state of the inputs is the less positive level.)



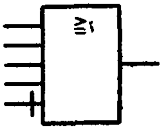
5.5.3 *OR with Negated Output (NOR)* — The output will stand at its 0-state if, and only if, at least one input stands at its defined 1-state.



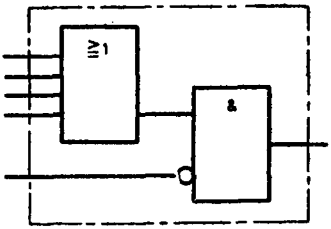
5.5.4 *NOR with One Negated Input*



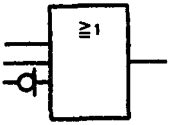
5.5.5 *OR with Inhibiting Input*



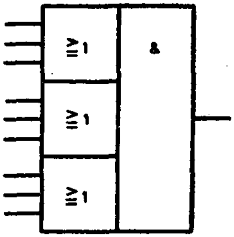
This is an abbreviated form of :



5.5.6 *OR With Negated Inhibiting Input*



5.5.7 Three OR's independent of each other but connected to an AND.



6. DEPENDENCY NOTATION

6.1 Explanation

6.1.1 The dependency notation is a means for obtaining simplified symbols for complex elements by denoting the relationship between inputs, outputs or inputs and outputs, without actually showing all the elements and interconnections involved. Apart from its use in complex elements, the dependency notation should not be used to replace the symbols for combinative elements.

6.1.2 The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

6.1.3 In the convention for the dependency notation use shall be made of the terms 'affecting' and 'affected'. In the case that it is not evident which inputs or outputs shall be considered as being the affecting or the affected ones the choice may be made in any convenient way.

6.1.4 Because of the existence of feedback in some complex elements, outputs sometimes have an effect on inputs and other outputs. For the sake of simplicity the following text refers to 'affecting inputs' only but it should be understood that the recommended notation applies to affecting outputs also. In this case the action of an affecting output is that obtained before the application of a negation or polarity indicator.

6.2 Convention — The dependency notation is accomplished by:

a) Labelling the input affecting other inputs or outputs with a particular symbol denoting the relationship involved followed by an identifying number;

b) Labelling each input or output affected by that affecting input with that same number.

c) Additional inputs or outputs having the same number with the bar over it are affected by the negated state of that affecting input (*see* **6.4.5**).

NOTE 1 — Where the affected input or output already has a label, denoting its function, this label will be prefixed by that number.

NOTE 2 — Two affecting inputs labelled with different symbols shall not have the same numerical suffix.

NOTE 3 — If an input or output is affected by more than one affecting input, then the identifying numbers of each of the affecting inputs shall appear in the label of the affected ones, separated by commas.

NOTE 4 — The left-to-right order of these identifying numbers is the same as the sequence of the affeting relationships.

NOTE 5 — If the labels denoting the functions of affected inputs or outputs are elsewhere defined to be numbers, then the identifying numbers to be associated with both affecting inputs and affected inputs or outputs shall be replaced by another character selected to avoid ambiguity.

NOTE 6 — An affecting input has only an effect on the corresponding affected inputs and outputs of the element.

6.3 AND- and OR-Dependency

6.3.1 *AND-Dependency* — The symbol denoting an AND-relationship between the affecting and affected inputs or outputs (an AND-dependency) is the letter G.

If two affecting inputs marked G have different identifying numbers, they stand in no relation to each other.

If, and only if, they have the same identifying number, they stand in an AND-relation to each other.

6.3.2 OR-Dependency — The symbol denoting an OR-relationship between the effecting and affected inputs or outputs (an OR-dependency) is the letter V.

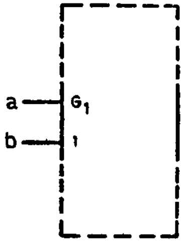
If two affecting inputs marked V have different identifying numbers, they stand in no relation to each other.

If, and only if, they have the same identifying number, they stand in OR-relation to each other.

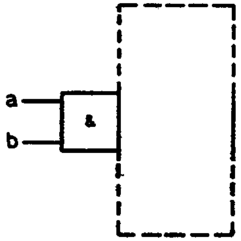
6.4 Illustrations of the Concept

Symbol *Description* *Explanatory Diagram*

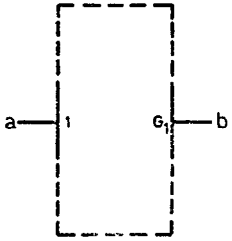
6.4.1



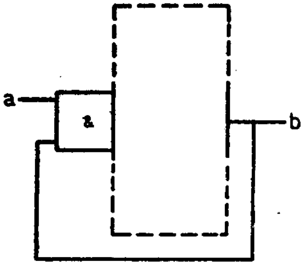
Input affecting another input (AND-relation).



6.4.2

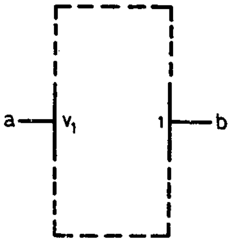


Output affecting an input (AND-relation).

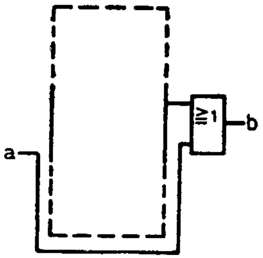


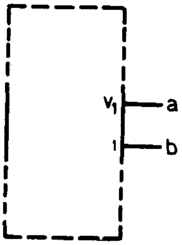
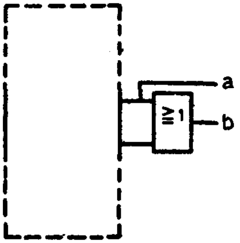
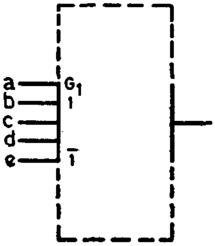
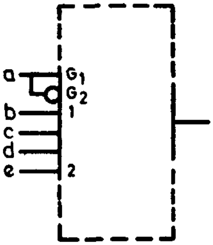
NOTE — If the symbol represents an arrangement of combinative elements, this method should not be used to depict sequential behaviour.

6.4.3



Input affecting an input (OR-relation).



	Symbol	*Description*	*Explanatory Diagram*
6.4.4		Output affecting another output (OR-relation).	
6.4.5		Use of negation in dependency notation.	

Further examples of the use of dependency notation will be found in **8.6**.

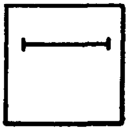
For some specific applications, *see* **8.3.15** and examples **8.10.3** and **8.11.2**.

7. DELAY ELEMENTS

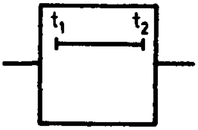
7.1 Explanation — An element in which each transition at the input causes one, and only one, delayed transition at the output.

7.2 Delay Element

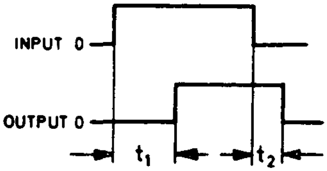
General symbol



7.3 Delay Element with Delay Times Specified — The transition from the 0-state to the defined 1-state at the output occurs after a delay of t_1 with reference to the same transition at the input. The transition from the defined 1-state to the 0-state at the output occurs after a delay of t_2 with reference to the same transition at the input.



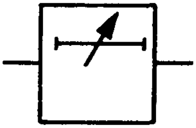
Example in positive logic where $t_1 > t_2$:



NOTE — t_1 and t_2 may be replaced by the actual delays, expressed in seconds, word units, or digit units and may be placed inside or outside the outline. If the two delays are equal, it is sufficient to insert one value only.

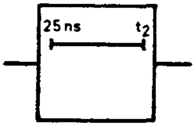
Unless otherwise stated the time (if quoted) are assumed to be nominal.

7.4 Variable Delay Element

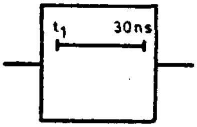


7.5 Examples of Use of Delay Elements

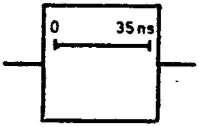
7.5.1 The delay pertaining to the output transition from the 0-state to the defined 1-state is specified (25 *ns*).



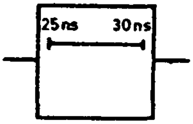
7.5.2 The delay pertaining to the output transition from the defined 1-state to the 0-state is specified (30 *ns*).



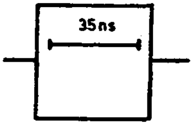
7.5.3 The transition from the 0-state to the defined 1-state is not delayed, and the transition from the defined 1-state to the 0-state is delayed by 35 *ns*.



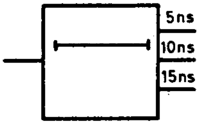
7.5.4 The transition from the 0-state to the defined 1-state is delayed by 25 *ns*, and the transition from the defined 1-state is delayed by 30 *ns*.



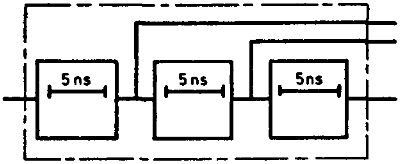
7.5.5 Both transitions are delayed by 35 *ns*.



7.5.6 Tapped delay element.



or

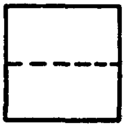


8. SEQUENTIAL ELEMENTS

8.1 Bistable Elements

8.1.1 A bistable element is a binary sequential logic element with two stable states.

8.1.2 *General Symbol — See also* **8.5.**



NOTE 1 — The information flows parallel to the broken line. This line need not be placed across the centre of the rectangle.

NOTE 2 — Outputs of the same type are placed at the same part of the symbol.

NOTE 3 — Two outputs, or groups of outputs, placed at opposite sides of the broken line are complementary.

8.1.3 *Rule* — If an input takes on its defined 1-state, the output placed at the same part of the symbol will take on its defined 1-state.

8.2 Inputs to Bistable Elements

8.2.1 *Convention*

a) All lines representing inputs may touch the symbol of the bistable element at any suitable place of the relevant part of the symbol.

b) The types of inputs shall be symbolized by a letter or figure or a group of letters or figures.

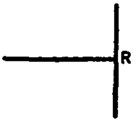
c) An input line function letter may be associated with another letter or number to indicate that the input is further dependent for its action on another input (dependency notation, **6.1** to **6.3**). This second input shall generally be labelled *G* or *C* and may be related to the first input by a letter or number.

d) Several inputs of the same type can be combined by an appropriate symbol such as AND, OR in order to act on a bistable.

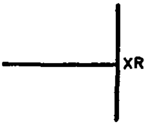
NOTE — If this operation is OR, it is unnecessary to show a symbol or to use dependency notation.

8.3 Examples of Inputs

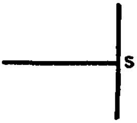
8.3.1 *Forcing Static R Input* — When the R input takes on its defined 1-state, it imposes the 1-state on the output placed at the same part of the symbol. This is defined as the 0-state of the bistable element. The return of the input to its 0-state produces no action.



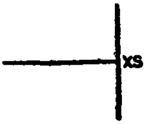
8.3.2 *Preparatory Static R Input* (subordinate to a command input X)



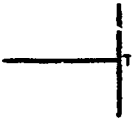
8.3.3 *Forcing Static S Input* — When the S input takes on its defined 1-state, it imposes the 1-state on the bistable element. The return of the input to its 0-state produces no action.



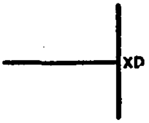
8.3.4 *Preparatory Static S Input* (subordinate to the command input X)



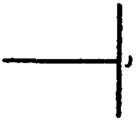
8.3.5 *T Input* — Each time the T input takes on its defined 1-state, it produces change-over (complementing action) of the bistable element. The return of the T input to the 0-state produces no action.



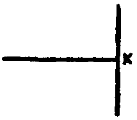
8.3.6 *D Input* — This is an input of which the action is subordinate to a command input X, and of which the two possible states are reproduced and stored by the bistable element.



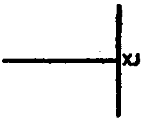
8.3.7 *J Input* — Forcing input analogous to the S input, but for which the combination $J.K = 1$ is defined, and causes the bistable element to change to the complementary state.



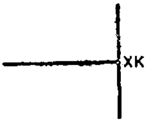
8.3.8 *K Input* — Forcing input analogous to the R input, but for which the combination $J.K = 1$ is defined, and causes the bistable element to change to the complementary state.



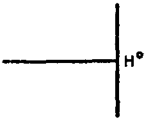
8.3.9 *Preparatory J Input* (subordinate to the command of input X)



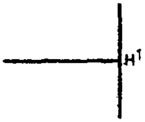
8.3.10 *Preparatory K Input* (subordinate to the command of input *X*)



8.3.11 *Holding Input for the 0-state* — The H° input maintains an existing 0-state of the bistable element. It has no influence on the 1-state of the bistable element.



8.3.12 *Holding Input for the 1-state* — The H^1 input maintains an existing 1-state of the bistable element. It has no influence on the 0-state of the bistable element.



NOTE — In symbols, **8.3.2**, **8.3.4**, **8.3.8**, **8.3.11** and **8.3.12** the *X* shall be replaced by the letters or figures required by dependency notation.

8.3.13 *C Input and Control Dependency*

a) The control-dependency denoted by the letter *C*, is used for squential elements in the case where more than a simple AND-dependency is implied. It is an extension of dependency notation (*see* **6**).

b) If a *C*-input stands at its defined 1-state, then the inputs affected by this *C*-input have their normally defined effect on the function of the element, provided that no other inputs have an overriding and contradicting effect.

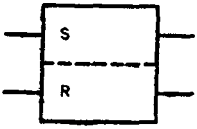
c) If a *C*-input stands at its 0-state, the inputs affected by this *C*-input have no effect on the function of the element and the outputs of the element remain at their existing states, provided that no other inputs have an overriding and contradicting effect.

d) If two *C*-inputs have different identifying numbers, they stand in no relation to each other.

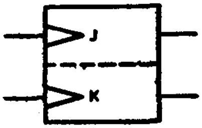
e) If, and only if, they have the same identifying number, they stand in an OR-relation to each other.

8.4 Examples of Bistable Elements

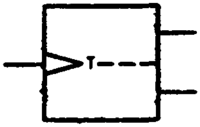
8.4.1 *RS Bistable Element* — If the two inputs take on different states or if both inputs take on their 0-states, the outputs stand at complementary states. If the two inputs take on different states, the output opposite the input which stands at its defined 1-state takes on its defined 1-state. If thereafter both inputs take on their 0 states, the outputs remain at their previous states. In the case when both inputs stand at their defined 1-states, and thereafter both inputs take on their 0-states simultaneously, the behaviour of the element is undefined.



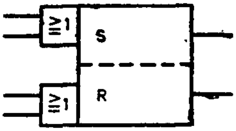
8.4.2 *JK Bistable Element* — The outputs always stand at complementary states. If one of the inputs takes on its defined dynamic 1-state, the output shown on the same part of the symbols take on its defined 1-state. If both inputs take on their defined dynamic 1-states simultaneously, the outputs are complemented. If both inputs take on their 0-states, the outputs remain at their previous states.

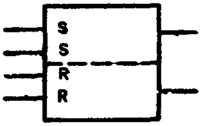


8.4.3 *T-Bistable Element (Binary Divider, Complementing Element)* — If the input takes on its defined dynamic 1-state, the states on the outputs are complemented. If the input takes on its 0-state, the outputs remain at their previous states.

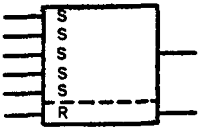


8.4.4 RS bistable element with two *R* inputs joined by an OR and two *S* inputs joined by an OR.





8.4.5 *RS* bistable element with five *S* inputs joined by an OR.



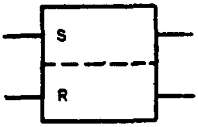
8.5 Deletion of the Broken Line in the Symbol for Bistable Element

8.5.1 To obtain a simpler representation, especially in memory arrays, and to obtain more space for additional text inside the symbol, the broken line in the symbol for a bistable element may be omitted if no ambiguity can arise.

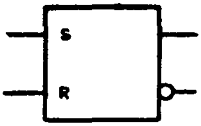
In such a case all outputs shall be shown by means of a negation or polarity indicator in the logic state or level which they will take on when the bistable element is in its defined 1-state (set state).

8.5.2 *Examples*:

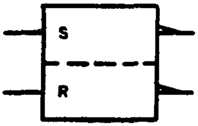
a)



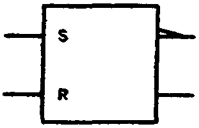
may be shown as:



b)



may be shown as:

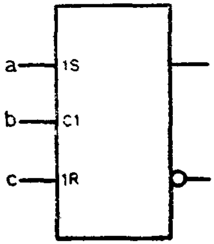


NOTE — Use of both forms (with and without broken lines) on one diagram is not recommended.

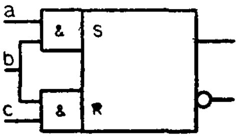
8.6 Examples of Bistable Elements Illustrating the Use of Dependency Notation

Symbol *Description* *Explanatory Diagram*

8.6.1

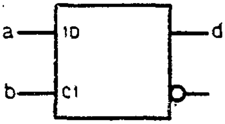


Input affecting two other inputs.

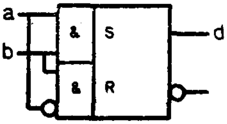


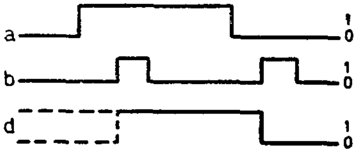
NOTE — In this case, use of the label *G* in place of the label *C* is equally valid.

8.6.2

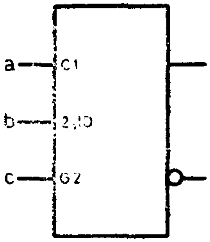


D bistable element

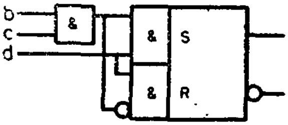




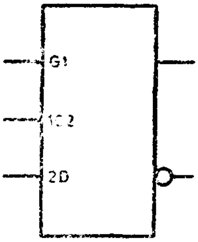
8.6.3



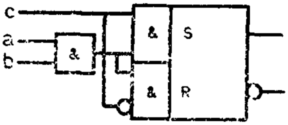
Input '*b*' is first affected by input '*c*' and then by input '*a*'.

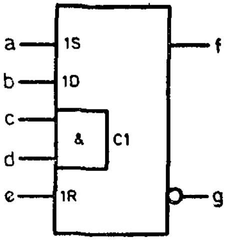
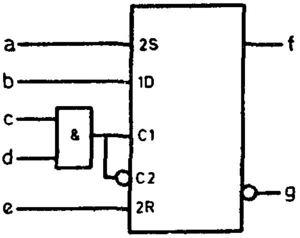


8.6.4

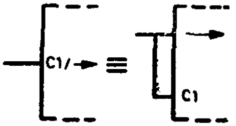


Input '*b*' affects input '*c*' and is itself affected by input '*a*'.

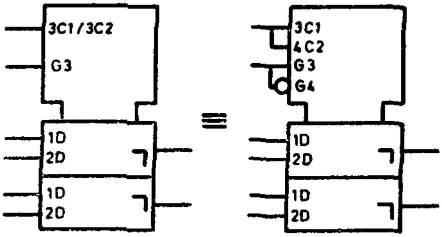


	Symbol	*Description*	*Explanatory Diagram*
8.6.5	 a b c d e 1S 1D & C1 1R f g	Use of negation in dependency notation.	 a b c d e 2S 1D & C1 C2 2R f g

8.6.6 *Input Having More Than One Function* — To aid in the representation of an input which has several labelled functional effects, the following form of abbreviation may be used:

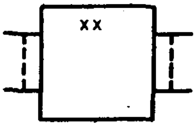


8.6.6.1 *Example of application*:



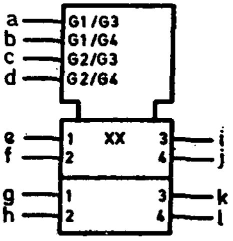
8.6.7 *Cross-Connected Switch* — The cross-connected switch, general symbol.

Representation of the control of the switch requires a particular application of dependency notation (*see* example).

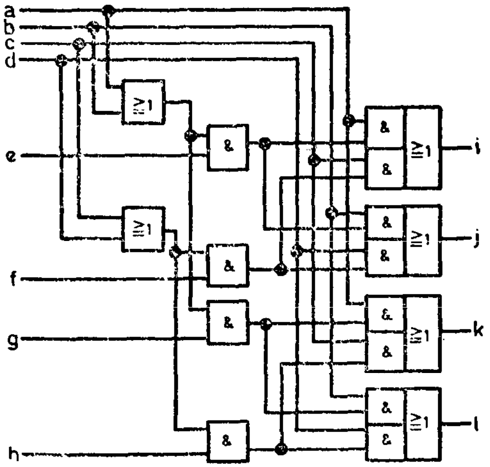


8.6.7.1 *Example* — Cross-connected switching arrangement.

If in a cross-connected switch a multiple gating input, having two G-labels separated by a '/', stands at its defined 1-state, the input labelled by the first numeral is connected to the output labelled by the second numeral. More than one connection path may be operated simultaneously.



Explanatory Diagram:



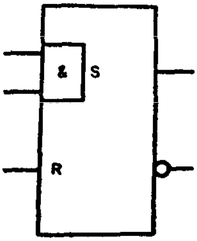
Note — If two or more data inputs are connected to one output, then they stand in an OR-relation. Otherwise there is no relation between the several data inputs.

8.7 Logic Symbols Inside Other Logic Symbols (Embedded Symbols)

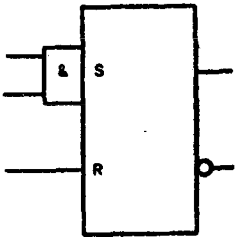
8.7.1 Any logic symbol, including the various distributed (wired) connections, may be placed inside another logic symbol if the relationship between the two, as established either by position or by internal connection lines, may be unambiguously interpreted.

8.8 Examples:

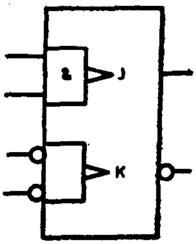
8.8.1



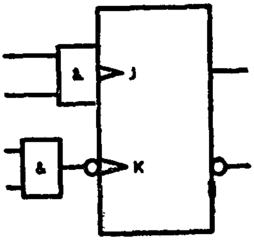
is functionally equivalent to:



8.8.2



is functionally equivalent to:

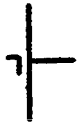


8.9 Representation of the Postponement of the Change of State of the Output

8.9.1 When the change of state of an output is postponed until the input signal which initiates the change returns to its initial state, this effect may be shown by labelling the output line with the symbol of **8.9.3**.

8.9.2 Where this symbol is shown without prefix it may be assumed to relate by convention to the *C* inputs only if the effect is related to other types of inputs (such as *S*, *R*, *G*, etc) then the labels of all applicable inputs (including the *C* inputs) shall be shown in full as a prefix to this symbol.

8.9.3 *Postponed Output Symbol* — Output of which the change of state is postponed until the input signal which initiates the change returns to its initial state.

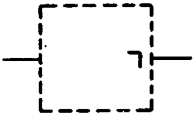


Note — Care should be taken that this symbol is a right angle, to avoid confusion with other symbols, for example, the number '7'.

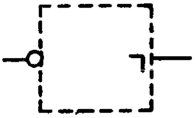
8.10 Examples — If there are no other inputs with an overriding effect, the transition at the output only takes place when the input changes:

8.10.1 In a system using the negation indicator

(from 1 to 0)

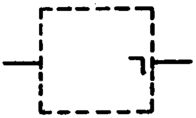


(from 0 to 1)

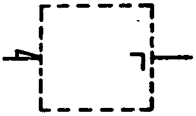


8.10.2 In a system using the polarity indicator

{ from more positive to less positive }



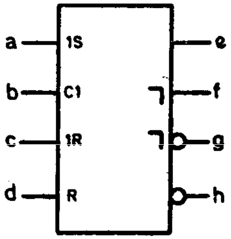
{ from less positive to more positive }



8.10.3 A master-slave combination of two bistable elements.

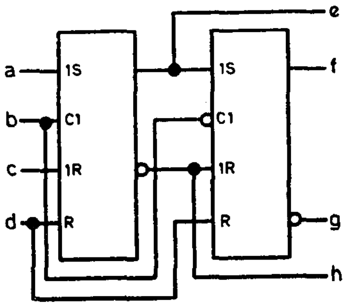
a) The two symbols shown are equivalent.

b) When input *d* takes on its defined 1-state, the outputs *g* and *h* take on their defined 1-states and the outputs *e* and *f* take on their 0-states. As long as input *d* stands at its 0-state, the function of the element is determined by the other inputs.



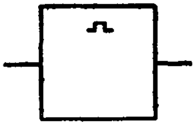
c) When input *b* stands at its defined 1-state, outputs *f* and *g* retain their previous states and outputs *e* and *h* act as those of an *RS* bistable element (*see* symbol **8.4.1**) under the control inputs *a* and *c*.

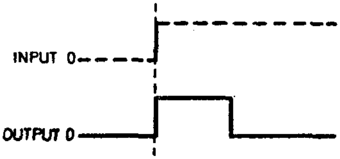
d) When input *b* retains to its 0-state, the outputs *e* and *h* retain their present states, outputs *f* and *g* assume the states of outputs *e* and *h* respectively.



8.11 Monostable Element — This is a binary sequential element with one, and only one, stable state.

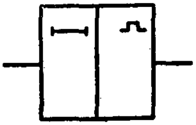
8.11.1 *Monostable Element, Single Shot* — The output will change to its defined 1-state only when the input changes to its defined 1-state. The output will remain in its defined 1-state for a period of time which is characteristic of the particular device, independent of the duration of the input variable.

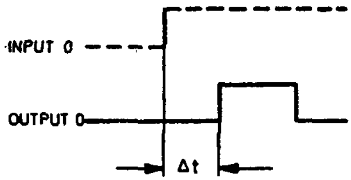




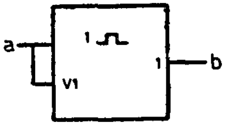
8.11.2 *Examples*:

a) Delayed monostable element, delayed single shot.

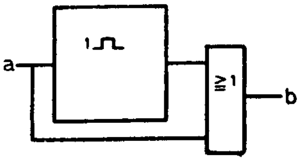




b) Monostable element, single shot, having an OR-grated output, shown with dependency notation.

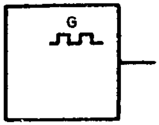


Explanatory diagram

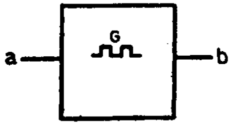


8.12 Astable Element — This is a binary sequential element with no stable state.

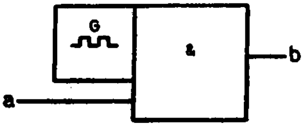
General symbol:



8.13 Controlled Astable Element



Explanatory diagram:



NOTE — In these symbols the *G* is the qualifying symbol for generator. If the waveform is evident these symbols may be shown without the waveform symbol

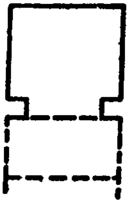
9. SYMBOLS FOR COMPLEX FUNCTIONS

9.1 Common Control Block

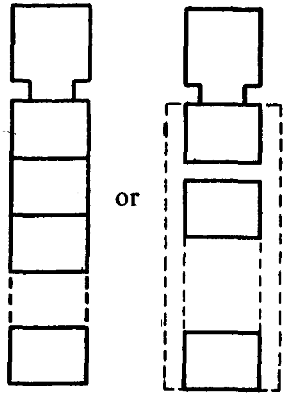
9.1.1 In an array of related elements it often occurs that some inputs are individual to one element and other inputs are common to all or some of the elements.

9.1.2 In order to reduce the space required on a diagram, to reduce line congestion and to obtain a clearer representation, the inputs which are common to all elements of the array need not be drawn connected to all individual elements, but only to a special symbol placed at one end of the array. This symbol is called the *Common Control Block*.

9.1.3 *Common Control Block*



Common Control Block	All common input lines should be connected to this part
Array of related elements	The individual lines of particular elements are connected to this part



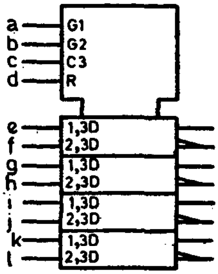
NOTE 1 — The right hand representation may be used in those cases where the output-input interconnections between elements of the array should be shown.

NOTE 2 — An input which is common to all elements shall be labelled at common control block in the same manner as it would have been in the individual element.

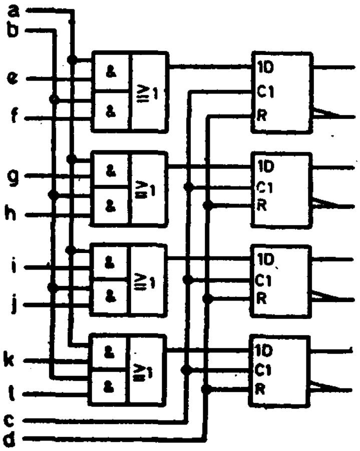
NOTE 3 — In some arrays, often those to which the common control block is applied, there exists two directions of information flow within the combination of elements. Hence the general rule of **3.4** does not apply.

9.2 Example of the Use of the Common Control Block — Register with an array of gated *D* bistable elements.

Symbol



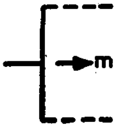
Explanatory Diagram



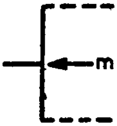
9.3 Shift Registers and Counters

9.3.1 *Shifting and Counting Inputs*

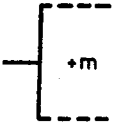
9.3.1.1 *Shifting input* — Each time this input takes on its defined 1-state, the information contained in the register will be shifted *m* positions from right left to right or from top to bottom.



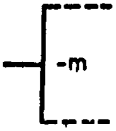
9.3.1.2 *Shifting input* — Each time this input takes on its defined 1-state, the information contained in the register will be shifted *m* positions from right to left or from bottom to top.



9.3.1.3 *Counting input* — Each time this input takes on its defined 1-state, the contents of the counter are increased by *m* units.



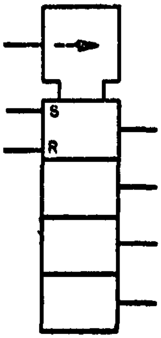
9.3.1.4 *Counting input* — Each time this input takes on its defined 1-state, the contents of the counter are decreased by *m* units.

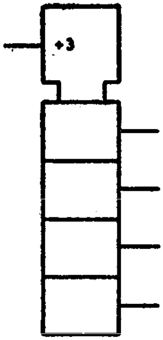


NOTE — '*m*' shall be replaced by the relevant value. If *m* = 1, '1' may be omitted.

9.4 Illustrations of the Concept

9.4.1 Four state shift register shifting one position from top to bottom each time the shifting input takes on its defined 1-state.

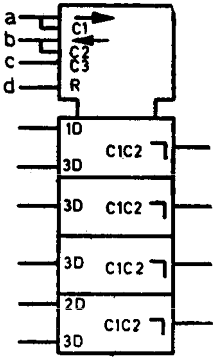




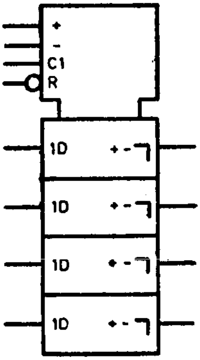
9.4.2 Four stage counter the contents of which are increased by 3 units each time the counting input takes on its defined 1-state.

NOTE 1 — In a counter the counting code may be shown in any convenient way, such that it does not interfere with other notations. If the code is not indicated, the counter is assumed to be a binary counter.

NOTE 2 — It is recommended that the section next to the common control block is the lowest order section.



9.4.3 *Bidirectional Shift Register* — Input '*a*' provokes shift action from top to bottom, input '*b*' from bottom to top and input '*c*' controls the parallel action. Input '*d*' is the common reset.

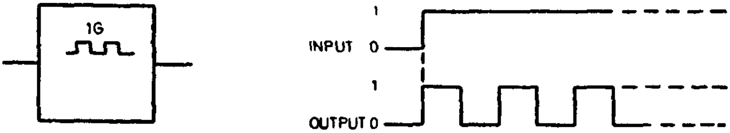


9.4.4 Four stage bidirectional counter with parallel loading and common reset.

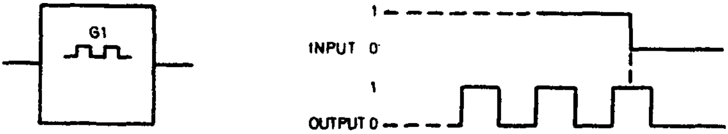
10. ASTABLE ELEMENTS

10.1 Synchronously Controlled Astable Elements

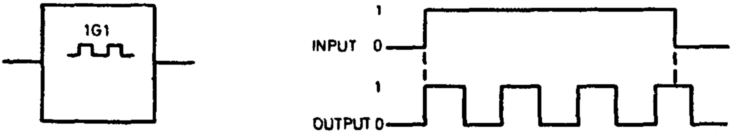
10.1.1 *Synchronously Starting Astable Element* — The output starts with a complete pulse when the input takes on its defined 1-state.

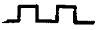


10.1.2 *Astable Element Synchronously Stopping After Completing the Last Pulse* — When the input returns to its 0-state, the output completes its final pulse and then remains at its 0-state.



10.1.3 *Synchronously Starting and Stopping Astable Element*



NOTE — In the symbols **10.1.1**, **10.1.2** and **10.1.3** the *G* is the qualifying symbol for generator. If the waveform is evident, these symbols may be shown without the waveform symbol 

11. COMMON OUTPUT ELEMENT

11.1 Explanation — In an array of related elements it often occurs that some outputs are individual to one element, and other outputs (called common outputs) depend on more than one element. Common outputs are represented as outputs of separate element symbols called *common output elements.*

The inputs of a common output element are considered to be:

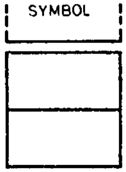
a) all non-negated outputs of the array, and

b) any inputs explicitly shown or indicated by dependency notation.

NOTE — A particular common output element may be such that the common output depends only on a portion of the non-negated outputs of the array.

The symbols of common output elements may be placed at one end of the array, separated from the array by two or more short strokes, as shown in **11.1.1**.

11.1.1 *Two Common Output Elements Attached to an Array*



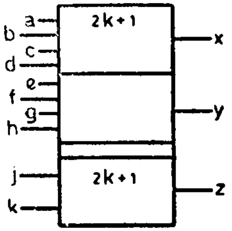
If a common control block is used, all common output elements should be placed:

a) either inside the common control block, and

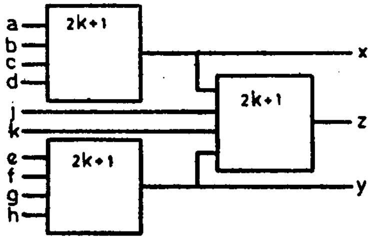
b) or at the end of the array opposite the common control block.

11.1.2 *Examples*

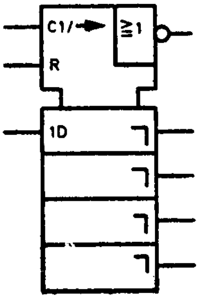
11.1.2.1 *Example of an odd parity generator using a common output element*



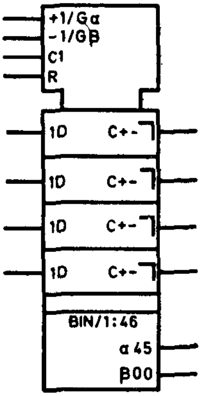
Explanatory Diagram



11.1.2.2 *Serial in/parallel out shift register with common output for the empty condition*



11.1.2.3 *Bidirectional counter with common outputs for carry and borrow*

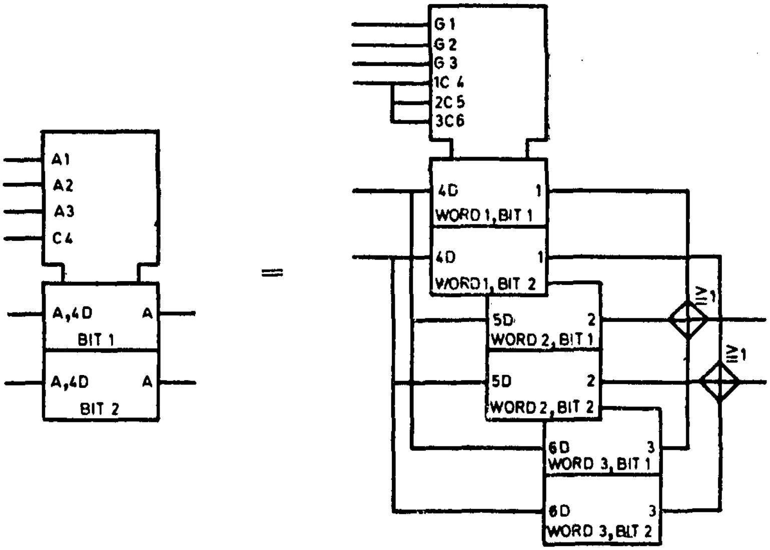


12. ADDRESS-DEPENDENCY

12.1 Explanation — Address-dependency is used to obtain a clear representation of those elements, particularly memories, which use address control inputs to select specified sections of a multi-dimensional array. The purpose of address-dependency is to allow a symbolic presentation of only a single general case of the sections of the array, rather than requiring a symbolic presentation of the entire array.

The symbol denoting address-dependency is the letter *A*.

Address-dependency allows the symbol on the left to depict the drawing on the right, which appears here only to illustrate the division into sections (*see* Figure below).



A stands for the complete group of identifying numbers. Hence the general rule for uniqueness of identifying numbers of dependency notation does not affect the assignment of address numbers.

If an *A*-input affecting a particular section of an array stands at its defined 1-state, then for that section:

a) all inputs affected by this *A*-input have their normally defined effect on the function of the element, and

b) all outputs affected by this *A*-input are enabled, providing that no other inputs have an overriding and contradicting effect.

If several sections are simultaneously selected by *A*-inputs standing at their defined 1-states, then the corresponding outputs of the selected sections stand in an OR-relation to each other.

If an *A*-input affecting a particular section of any array stands at its 0-state, then for that section:

a) all inputs affected by this *A*-input have no effect on the function of the element, and

b) all outputs affected by this *A*-input stand at their 0-state.

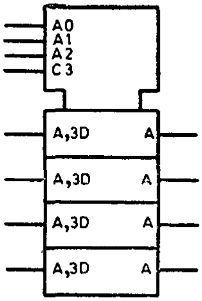
The inhibiting effect of an *A*-input standing at its 0-state takes precedence over the effect of any CONTROL-dependency (denoted by *C*), AND-dependency (denoted by *G*) or OR-dependency (denoted by *V*).

If there are several sets of address inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter denoting ADDRESS-dependency is 1*A*, 2*A*, ... instead of *A* (*see* for example Symbol under **12.2.3**).

12.2 Examples

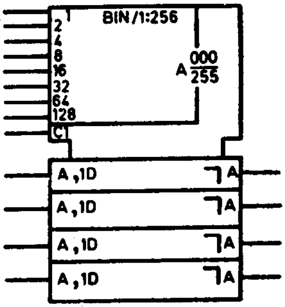
12.2.1 *3 Address-4 bit memory* (*symbol for a device with 3 sections*)

Symbol



12.2.2 *256 Address-4 bit memory (symbol for a device with 256 sections)*

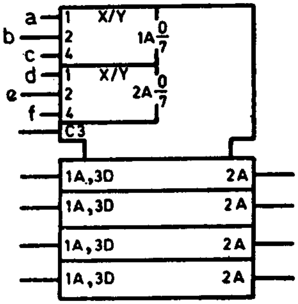
NOTE — The method of indicating the decoded address inputs in the example may also be used for other types of decoded gating inputs.



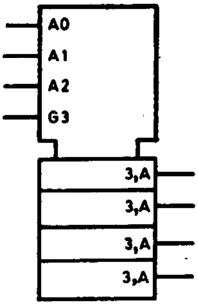
12.2.3 *8 Address-4 bit memory with independent address selection for writing and for reading*

Inputs *a*, *b*, and *c* select the data input address.

Inputs *d*, *e*, and *f* select the address for the output.

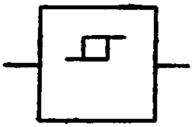


12.2.4 *3 Address-4 bit read only memory with gated outputs*



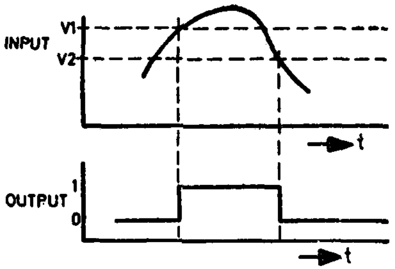
13. MISCELLANEOUS

13.1 Threshold Detector (Schmitt Trigger)



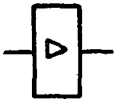
The output of a threshold detector will take on its defined 1-state only at such time that the input signal exceeds a specific threshold value (V_1) in the indicated direction. The output remains at its defined 1-state until such time that the input signal returns past a specific threshold value (V_2).

Explanatory graph:

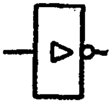


13.2 Amplifiers

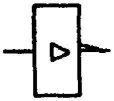
13.2.1 *Amplifier for Logic Diagrams* — The output will stand at its defined 1-state if, and only if, the input stands at its defined 1-state.



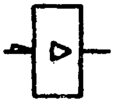
13.2.2 *Amplifier with Negation Indicator* — The output will stand at its 0-state if, and only if, the input stands at its defined 1-state.



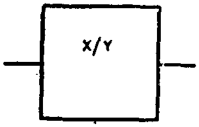
13.2.3 *Inverting Amplifiers* — The output will stand at the more positive level if, and only if, the input stands at its less positive level.



or



13.3 Signal Level Converter — The level references may be shown inside the symbol and shall replace *x* and *y* if confusion with the coder may arise.



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